Recent CGA/PBGA/QFN Package Testing

by

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Outline

- Packaging
  - Evolution
  - Single Packaging Trends
- NEPP CGAs
  - CGA IBM/Cu-wrapped Columns
  - BME Cap Evaluation
  - CGA 1272/1517 Cu-wrapped Columns TC results
- NEPP PBGAs
  - FPBGA Testing
  - FCBGA 1704 Testing
- NEPP QFN/BTC
  - BOK
  - No Testing
- Summary

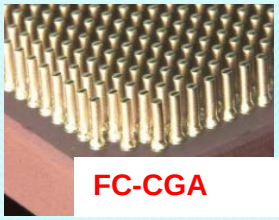
Packaging Evolution

- 1990s
  - TH well established in Hi-Rel
    - Concern on SMT leaded parts
  - SMT well established in Hi-end/Desktop computer
    - Concern on newly introduced PBGAs
- 2000s
  - PBGA/CGA use in Hi Rel
    - Concern on finer pitch/stack
  - CSP/QFN/Stack use in consumer/portable
    - Concern on 3D stack/HDI /Pb-free
- 2010s
  - PBGA/CGA wider use in Hi Rel
    - More Plastics//2.5D for FPGA/Concern on Pb-free
  - Pb-free use in consumer
    - Pb-free implement/Hi-end evaluated
- 2020s
  - PBGA >2000 I/O use in Hi Rel
    - FPBGA/stack/Pb-free?
  - iNEMI 2015 Roadmap & $$

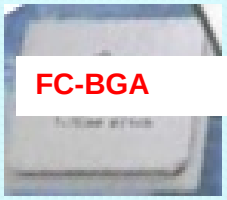
NEPP Activities

CGA/FCBA Testing
QFN: BOK

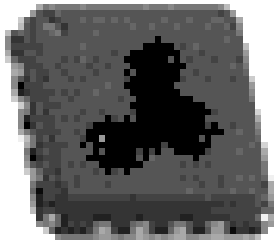
CGA 1144, 1509, 1752
IBM Column
CGA 1272 Six Sigma
CGA 1517 Six Sigma
Microcoil Spring



FCBGA
1704



BOK
QFN



CGA: Column Grid Array
FCBGA: Flip Chip Ball Grid Array
QFN: Quad Flat No-Lead
BOK: Body of Knowledge

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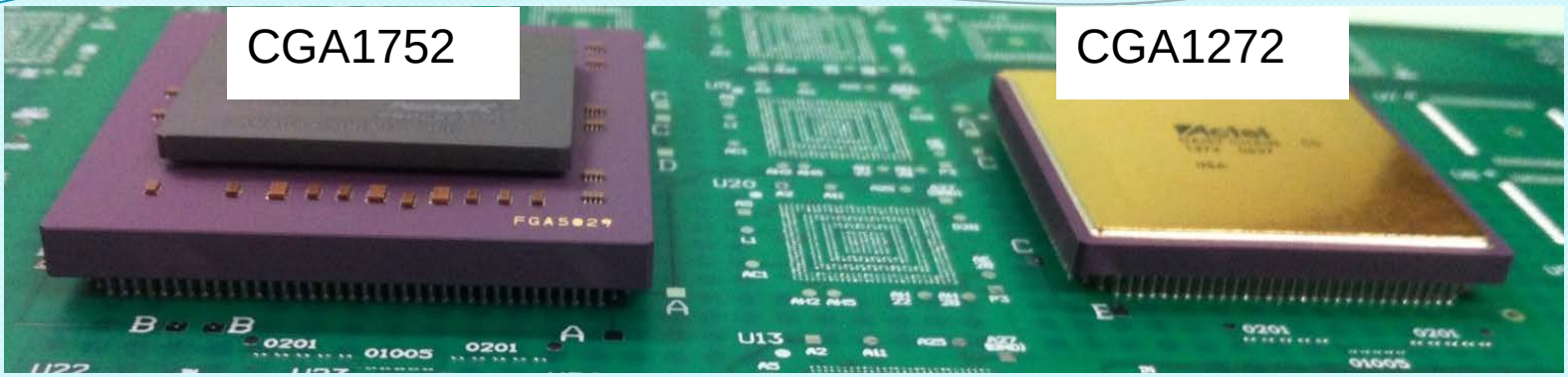
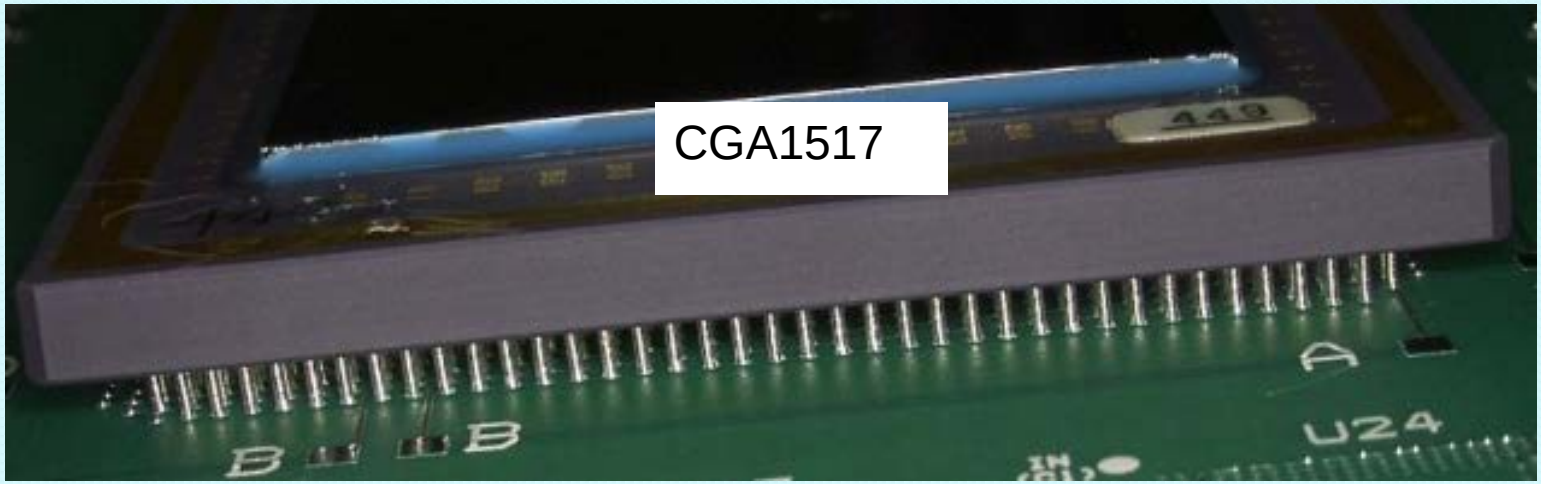
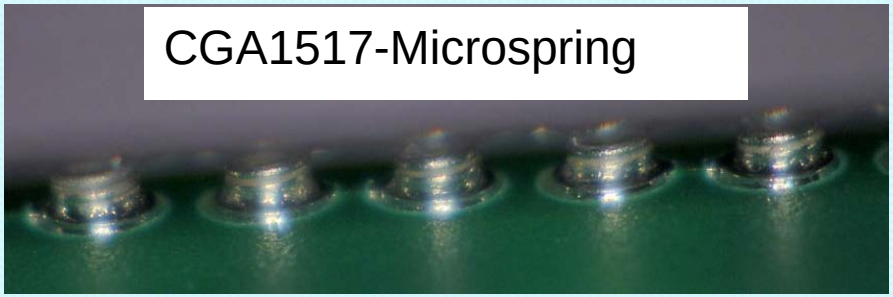
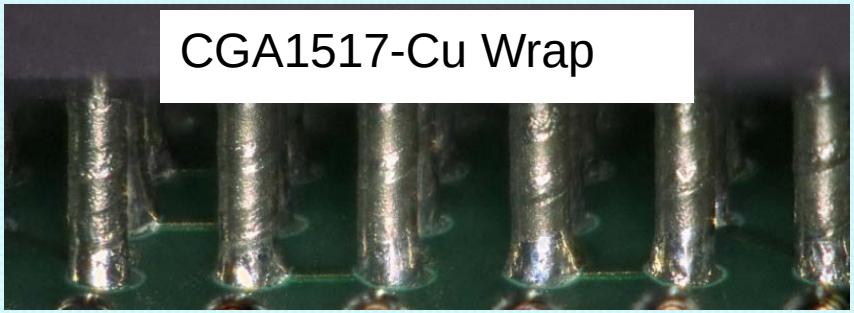
NEPP CGA Testing









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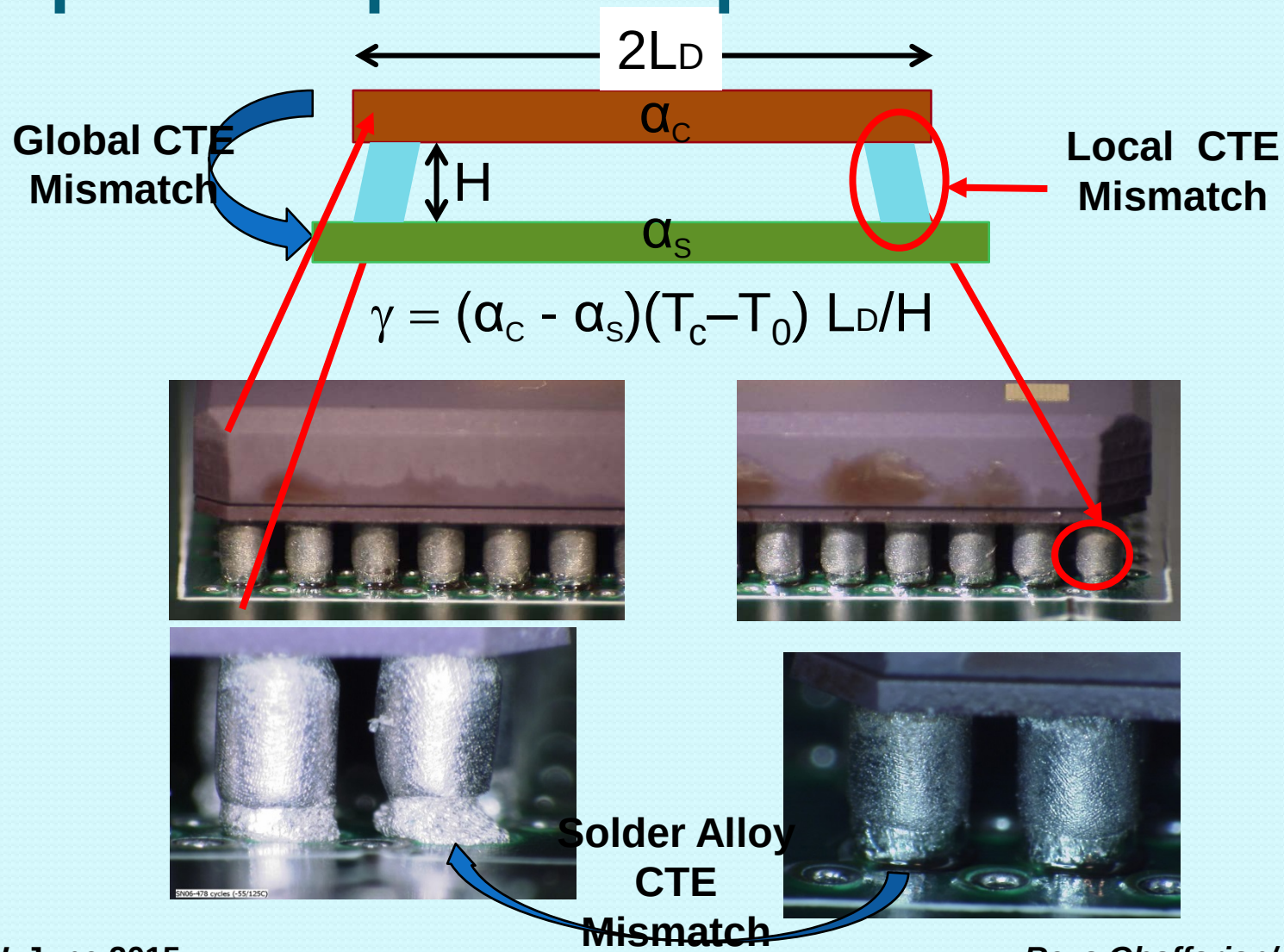
Reliability

Thermal Global/Local & Stake Interposer/Cap/Via/bump/Underfill/Heat Sink



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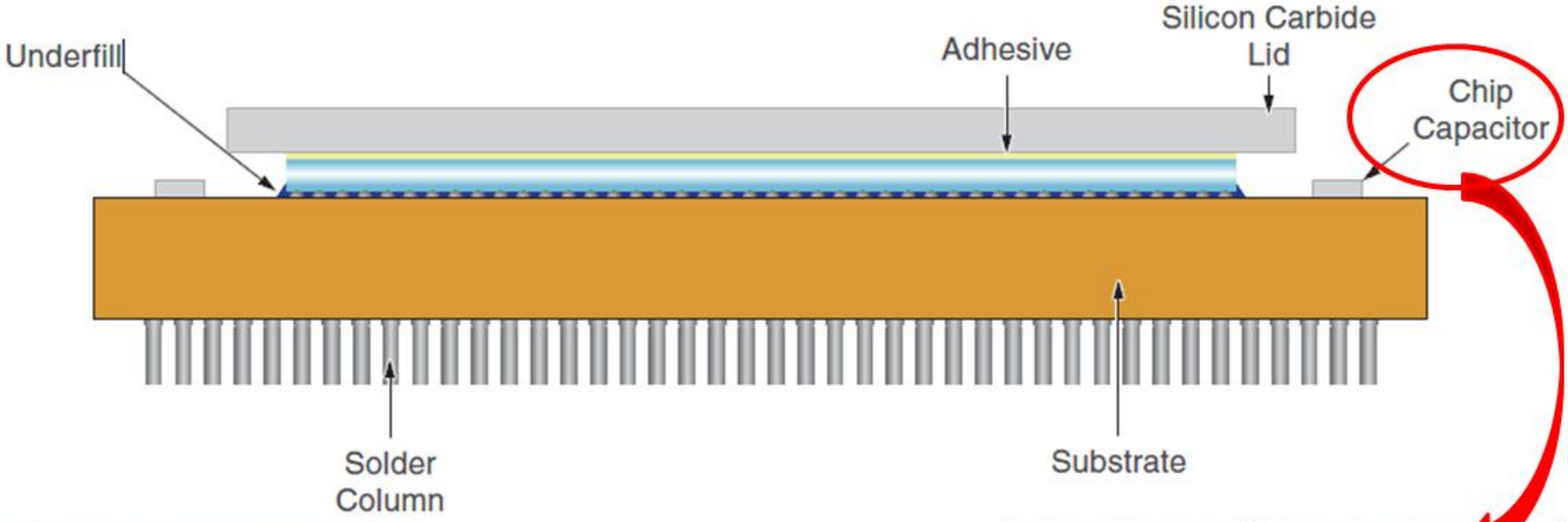
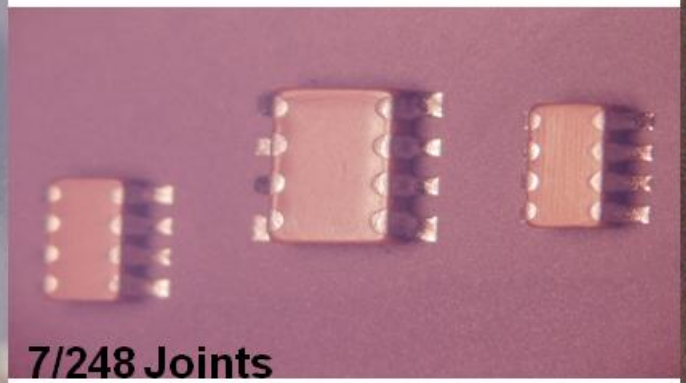
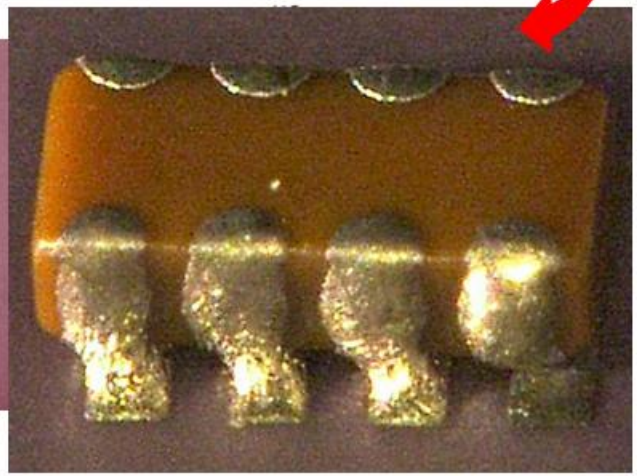
CGA 31 Caps







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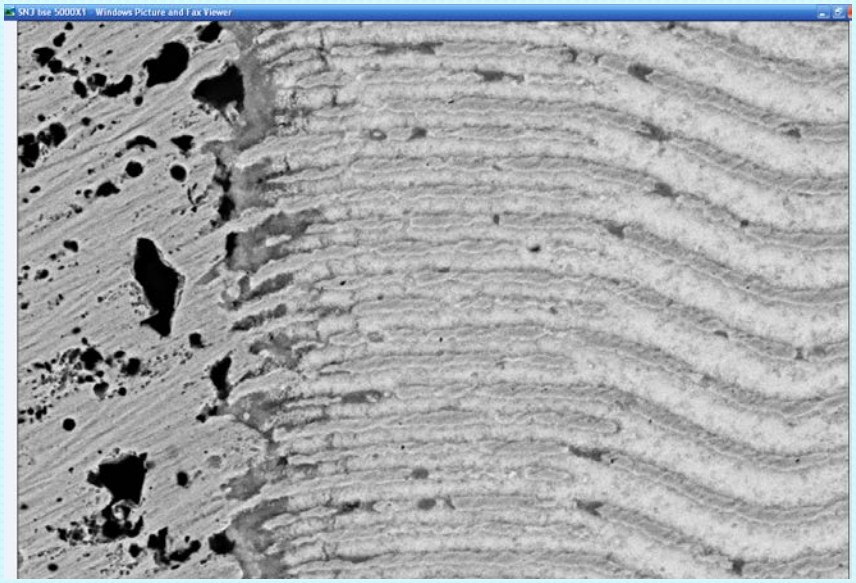
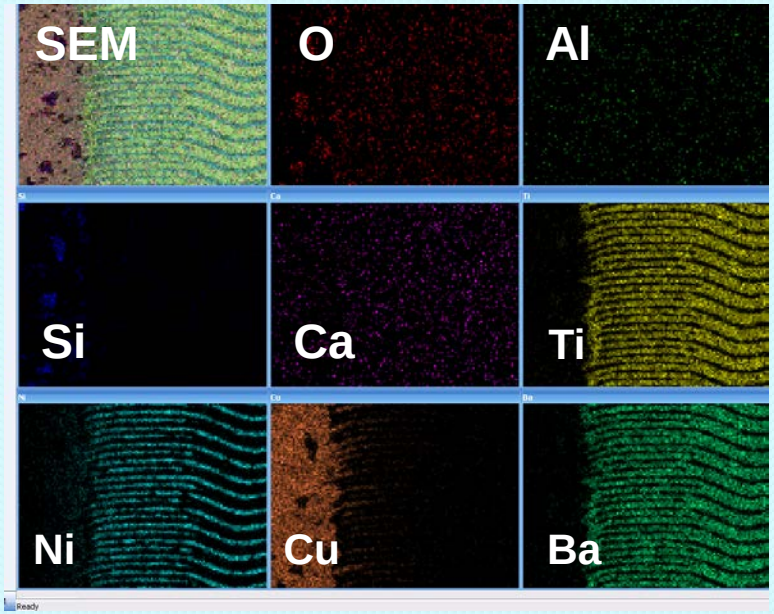
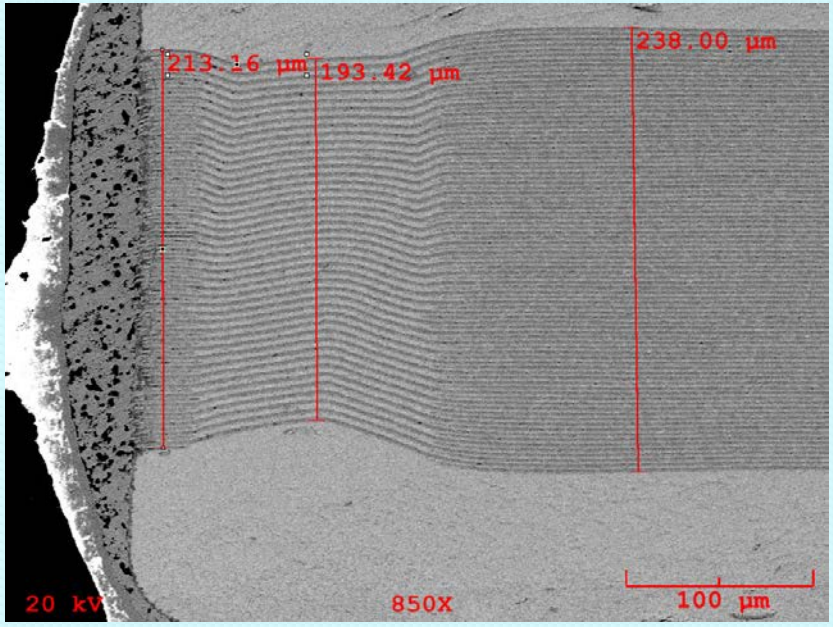
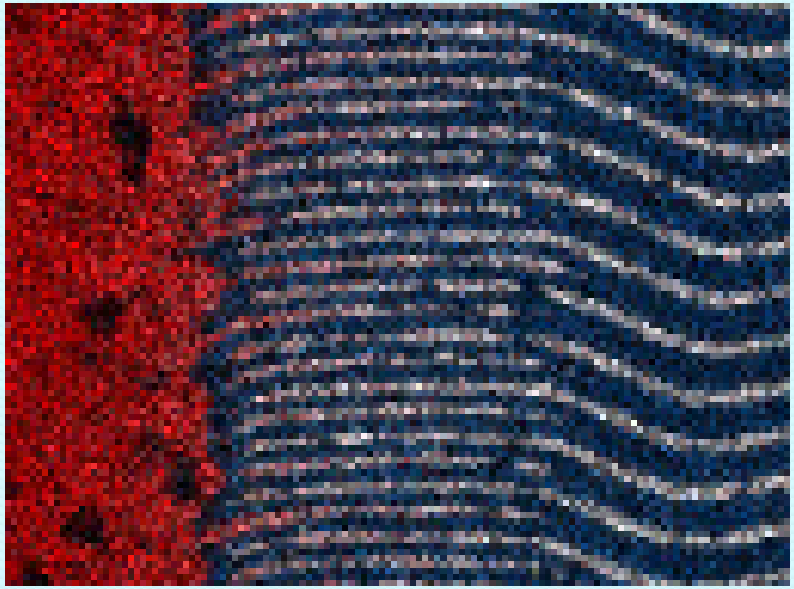
BME X-section & Elemental Map









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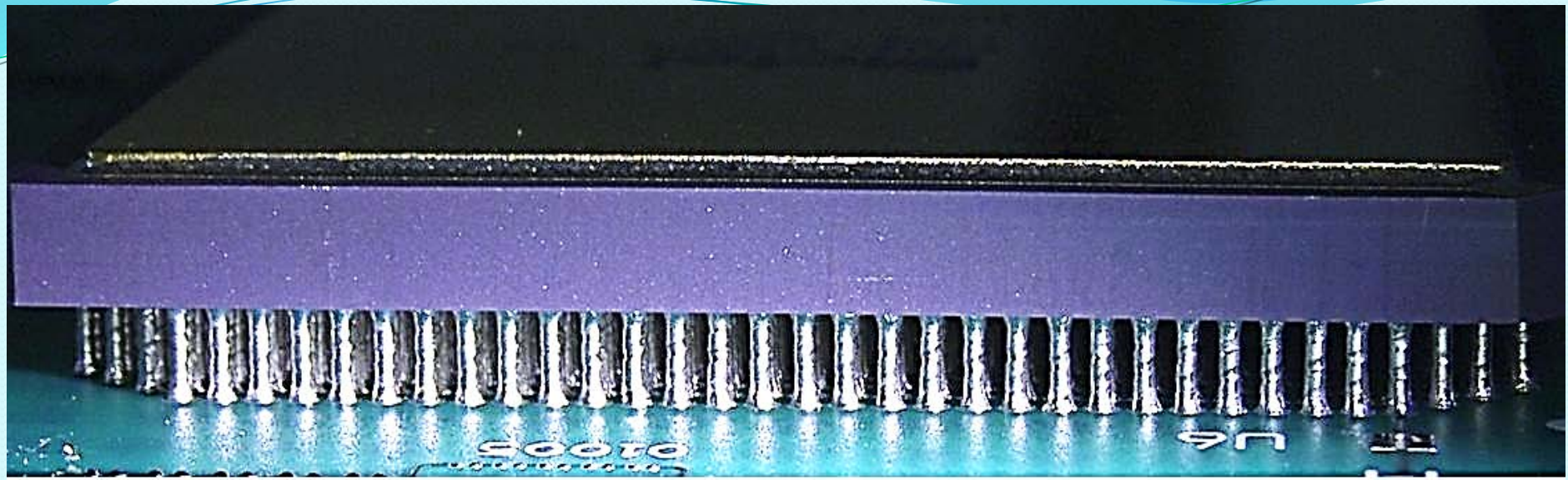
IPC 9701- TC Conditions

Table 1 Temperature cycling requirements specified in Table 4.1 of IPC 9701

Test Condition	Mandated Condition
Temperature Cycle (TC) Condition: ***TC1***	***0°C ↔ +100°C (Preferred Reference)***
TC2	–25°C ↔ +100°C
TC3	–40°C ↔ +125°C
TC4	–55°C ↔ +125°C
TC 5	-55 °C<-> 100°C
Test Duration	Whichever condition occurs FIRST: 50% ***(preferred 63.2%)*** cumulative failure (Preferred Reference Test Duration) or
Number of Thermal Cycle (NTC) Requirement: NTC-A	200 cycles
NTC-B	500 cycles
NTC-C	1,000 cycles (Preferred for TC2, TC3,and TC4)
NTC-D	3,000 cycles
NTC-E	***6,000 cycles (Preferred Reference TC1***)
Low Temperature Dwell	10 minutes
Temp. tolerance (preferred)	+0/–10°C (+0/–5°C) [+0/–18°F (+0/–9°F)]
High Temperature Dwell	10 minutes
Temp. tolerance (preferred)	+10/–0°C (+5/–0°C) [+18/–0°F(+9/–0°F)]

CGA 1272



CGA 1272- 100TC (-55/100°C)

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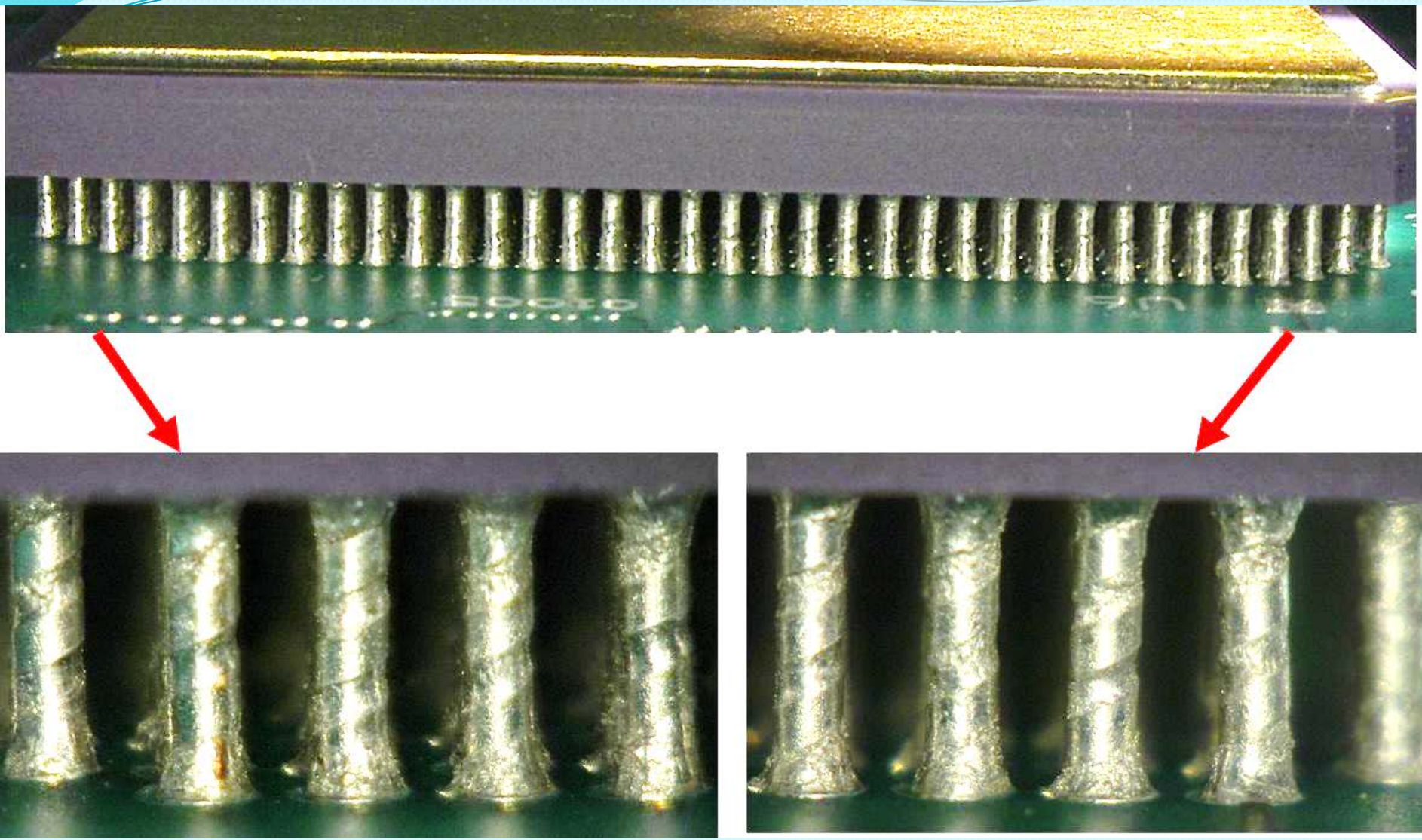
CGA 1272



CGA 1272- 500TC (-55/100°C)

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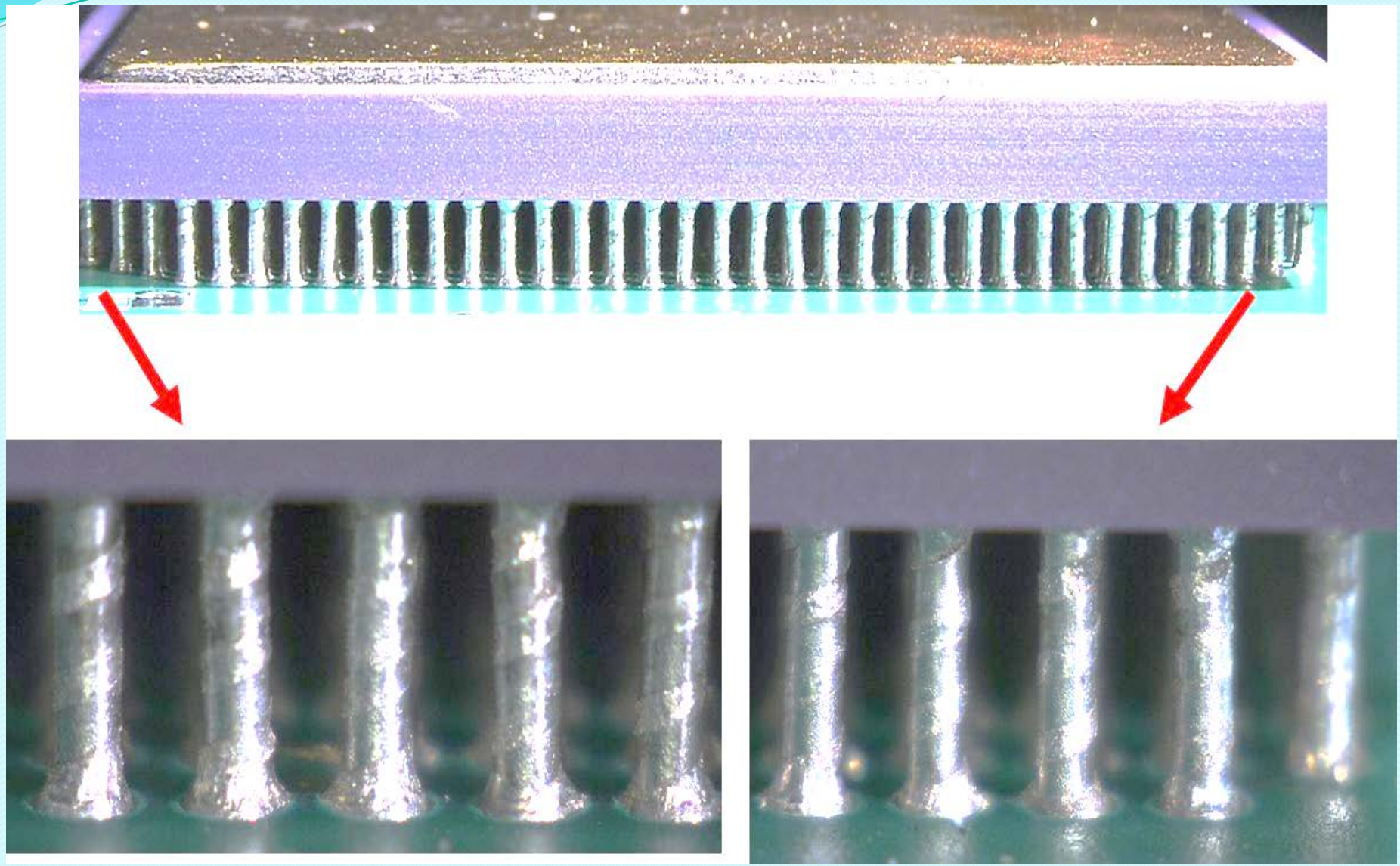
CGA 1272



CGA 1272- 500TC (-55/125°C)

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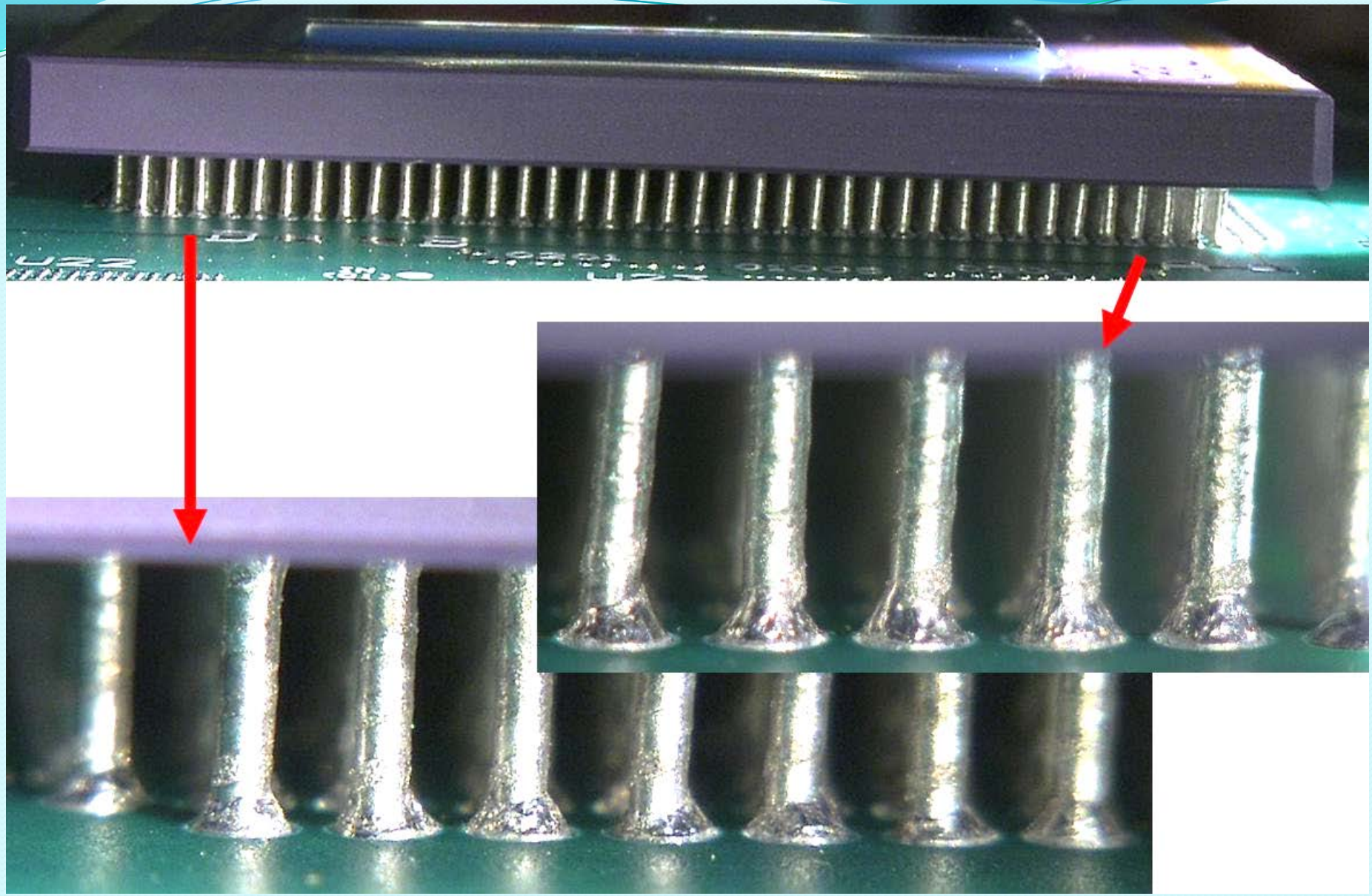
CGA 1517



CGA 1517- 500TC (-55/100°C)

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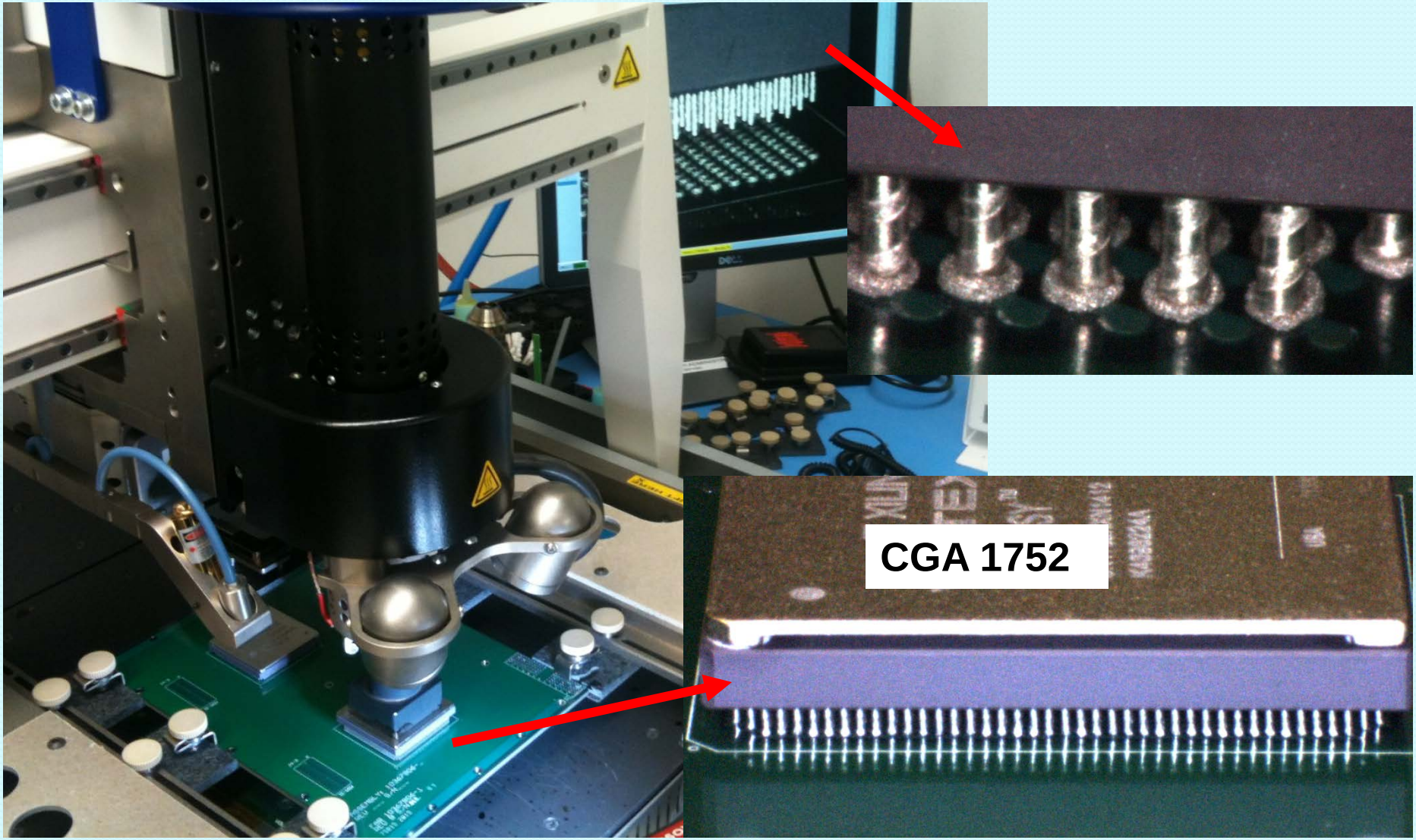
Recent CGA Activities

- Inspect CGA/review process
  - ETW presentations
  - Two day visit, but a week for agreement
- Voiding
  - CGA voiding
  - Reviewed process/solder paste
- Inspection/assembly daisy-chain parts
  - Use of tray, but individually sealed
  - Handling caused columns to bend
  - Process optimization
    - Needs controls for each assembly

New CGA 1752- Cu Wrap



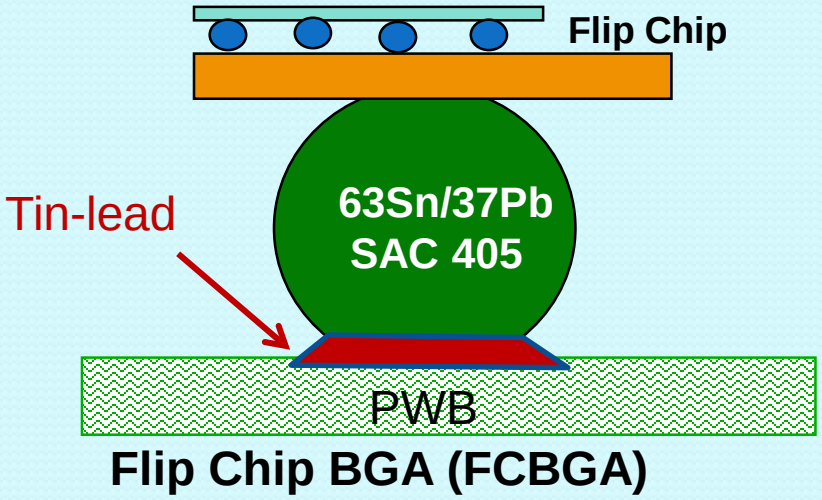
PBGA & FCBGA

- Limitation of PBGAs
  - Wire bonds only periphery
    - Solution: Tier wire bonding, still limit for higher I/Os
  - Higher speed need
    - No solution

- FCBGA advantages
  - Use area of die, larger I/Os than periphery
  - Higher speed
    - Short electrical path: Low capacitance, inductance, resistance
    - Accommodate higher I/Os >1000

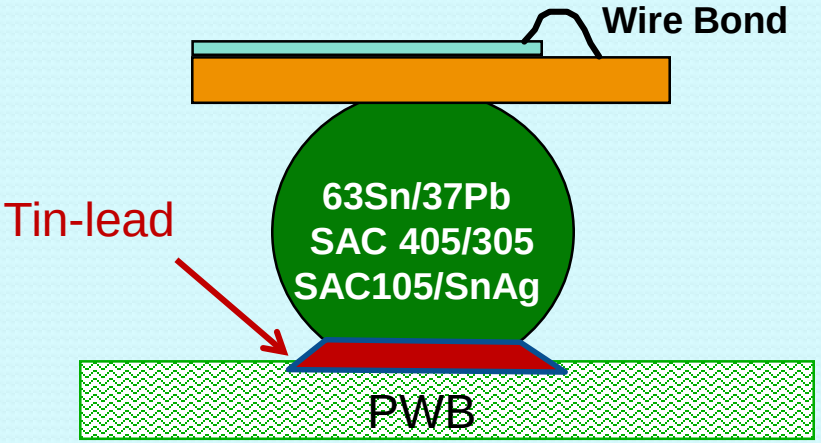
NEPP FCBGA Testing

- Flip Chip BGA
  - FCBGA 1704 I/O 1.0 mm pitch



Flip Chip BGA (FCBGA)

- BGA- Wire bond:
  - PBGA 676 I/O 1.0 mm /control
  - FPBGA 432 I/O 0.4 mm/state-of-the-art



Plastic BGA (PBGA)

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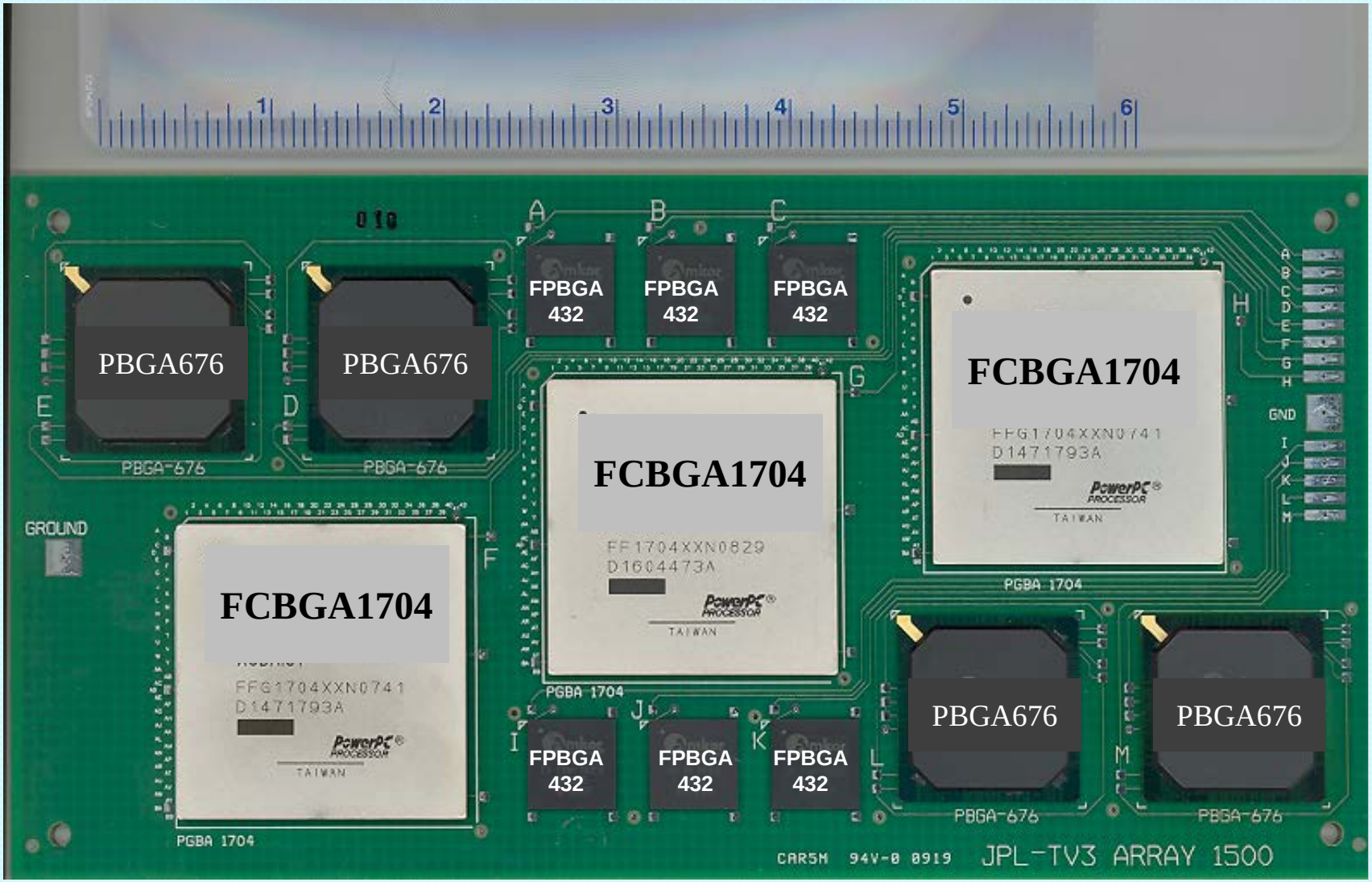
NEPP FCBGA Testing



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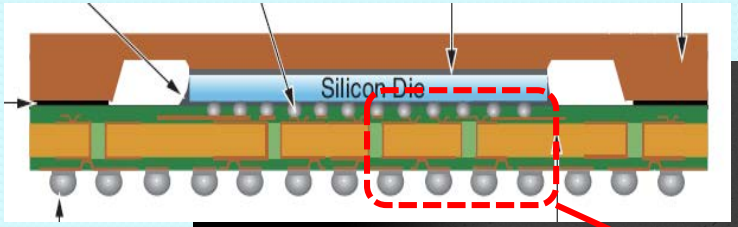
X-Section FCBGA 1704



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Package Volume

Package Style (Bn Units)	2010	2011	2016	CAAGR 2016/2011	% of IC 2016
DIP/SOT	5.3	4.3	3.9	-1.9%	1.4%
SO/TSOP/SOT	83.0	80.8	108.4	6.0%	37.8%
QFP/LCC	19.0	18.3	24.5	6.0%	8.6%
QFN	19.6	20.5	46.0	17.0%	16.1%
Wire Bond FBGA	8.0	8.2	12.6	8.9%	4.4%
Stacked FBGA	6.2	6.8	10.9	9.8%	3.8%
BOC	12.0	12.5	15.5	4.4%	5.4%
Wire Bond BGA	1.4	1.3	0.8	-7.9%	0.3%
COB (Wire Bond)	7.2	7.7	11.3	8.0%	3.9%
Flip Chip FBGA	0.8	1.6	8.1	39%	2.8%
Flip Chip BGA/PGA/LGA	1.1	1.1	1.6	7.1%	0.6%
DCA/WLCSP	12.9	14.5	29.2	15.0%	10.2%
COG/COF	8.6	9.2	13.7	8.3%	4.8%
Total Wire Bond	161.7	160.3	233.8	7.8%	81.6%
Total Flip Chip	23.4	26.4	52.6	14.8%	18.4%
IC TOTAL	**185.1**	**186.7**	**286.4**	**8.9%**	**100%**

World Wide Semiconductor Package Volume (billions of units) (iNEMI/Prismark)

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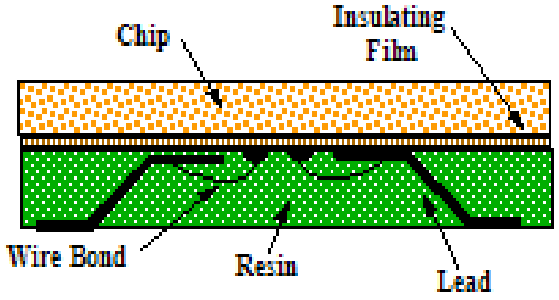
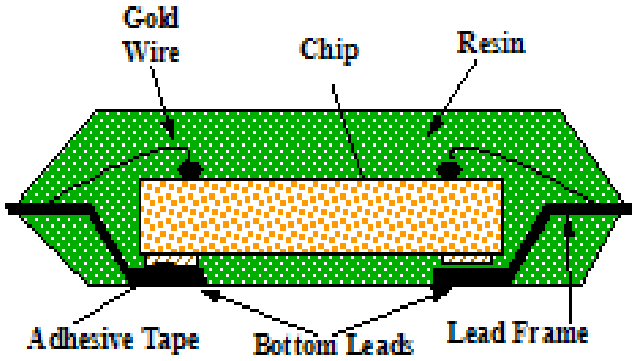
QFN/BTC

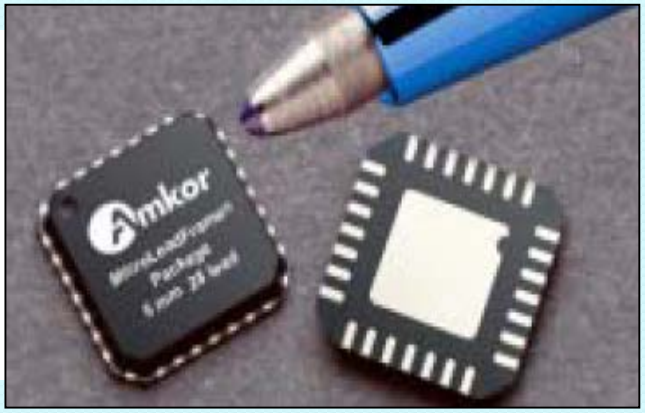


Lead On Chip
LOC



Ultra-Thin-Small-Outline
USON

MicroLead Frame®



QFN: Quad Flat No-lead
BTC: Bottom Termination Component

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C-QFN

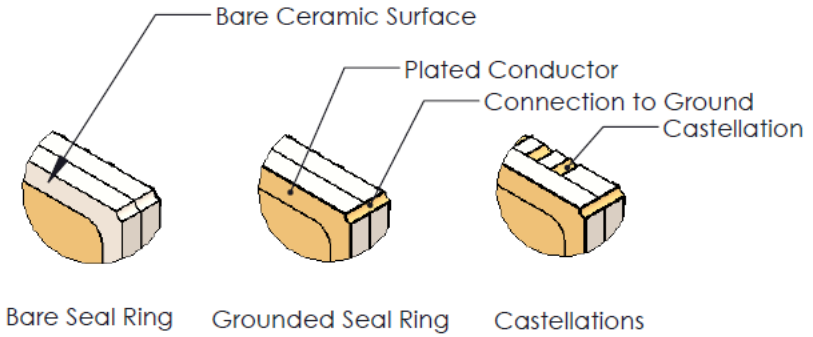
C-QFN Alumina Air Cavity Family

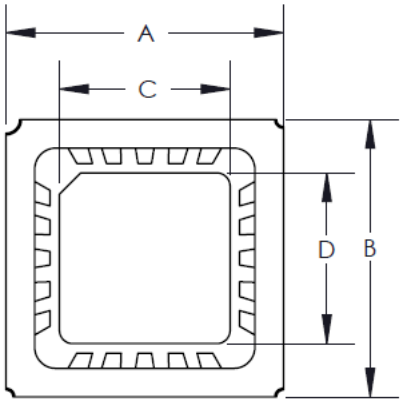
Features

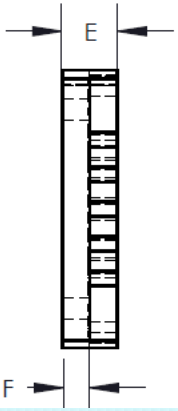
- High Temperature Co-Fire Alumina Body
- Low Loss Broadband Transitions
- Air Cavity
- Low Thermal Resistance
- JEDEC MO-220 Footprint
- 0.5 mm Lead Pitch

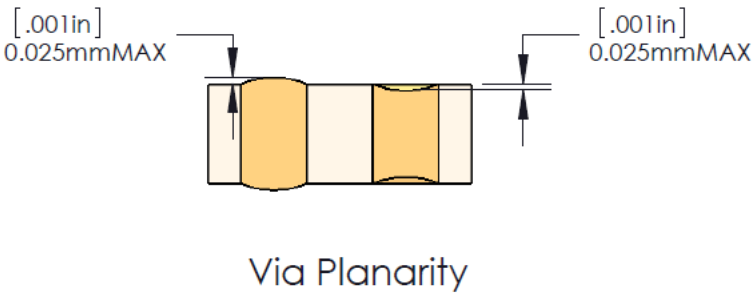
Options

- Grounded Seal Ring
- Castellated Pins
- Hermeticity
- NiAu or ENIG or ENEPIG Plating









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Summary

- CGA
  - Extensive test data
  - CN 1752 I/O with Cu-Wrap
- FCBGA
  - Extensive test data/Recent FCBGA1704 I/O
  - New test vehicle
    - FCBGA ~2000 I/O, WLP 1600 I/O, Pitch to 0.3, stack, more!
- QFN/BTC
  - BOK released
  - Lag industry in testing
- Others
  - Many: Stack, FPGA, WLP, embed, new interconnections
  - iNEMI

The **convergence of mobile phones with computing and entertainment** devices in effect enforces the further ramp of CMOS into SoCs (systems-on-chip), both in homogeneous and heterogeneous technologies. The classical mixed technologies in 2D SiP and MCP (multi-chip package) forms is now **evolving and growing to more of a 3D MCP** with a new set of electrical, mechanical and thermal challenges.

The 3D stacking of chips will be mostly dominated by **three key components: memory, application processor and communication silicon.** They will leverage through-silicon via **(TSV)** and through-mold via **(TMV)** in integrated, mixed technologies in single-package as well as chip-on-chip (CoC) and chip-on-interposer solutions over the next five-year horizon.

Of course, the commercial challenges associated with 3D stacking, especially in the world of memory integration, are expected to remain a significant barrier. Consignment, material, need for liquidity of memory size and even the supply chain and test challenges will remain the ramp barriers as they all impact the bottom line.

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